

# BGA7350

50 MHz to 250 MHz high linearity Si variable gain amplifier;  
24 dB gain range

Rev. 1 — 21 December 2011

Product data sheet

## 1. Product profile

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### 1.1 General description

The BGA7350 MMIC is a dual independently digitally controlled IF Variable Gain Amplifier (VGA) operating from 50 MHz to 250 MHz. Each IF VGA amplifies with a gain range of 24 dB and at its maximum gain setting delivers 17 dBm output power at 1 dB gain compression and a superior linear performance.

The BGA7350 Dual IF VGA is optimized for a differential gain error of less than  $\pm 0.1$  dB for accurate gain control and has a total integrated gain error of less than  $\pm 0.4$  dB.

The gain controls of each amplifier are separate digital gain-control word, which is provided externally through two sets of 5 bits.

The BGA7350 is housed in a 32 pins 5 mm × 5 mm leadless HVQFN32 package.

### 1.2 Features and benefits

- Dual independent digitally controlled 24 dB gain range VGAs, with 5-bit control interface
- 50 MHz to 250 MHz frequency operating range
- Gain step size: 1 dB  $\pm$  0.1 dB
- 18.5 dB power gain
- Fast gain stage switching capability
- 17 dBm output power at 1 dB gain compression
- 5 V single supply operation with power-down control
- Logic-level shutdown control pin reduces supply current
- Excellent ESD protection at all pins
- Moisture sensitivity level 2
- Unconditionally stable
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

### 1.3 Applications

- Compatible with W-CDMA / WiMAX / LTE base-station infrastructure / multi carrier systems
- Multi channel receivers
- General use for ADC driver applications



## 1.4 Quick reference data

**Table 1. Quick reference data**

$A\_EN = "1"$ ;  $B\_EN = "1"$  (VGA enabled). Typical values at  $V_{CC} = 5\text{ V}$ ;  $I_{CC} = 245\text{ mA}$ ; Tuned for  $f_{IF} = 172\text{ MHz}$ ;  $B = 28\text{ MHz}$ ;  $T_{case} = 25\text{ }^{\circ}\text{C}$ ; Differential input resistance matched to  $140\text{ }\Omega$ ; Differential output resistance matched to  $200\text{ }\Omega$ ; unless otherwise specified; see [Section 11 "Application information"](#).

| Symbol             | Parameter                             | Conditions                                     | Min  | Typ       | Max  | Unit     |
|--------------------|---------------------------------------|------------------------------------------------|------|-----------|------|----------|
| $V_{CC}$           | supply voltage                        | $V_{CC(A)} + V_{CC(B)}$                        | 4.75 | 5         | 5.25 | V        |
| $I_{CC}$           | supply current                        | $I_{CC(A)} + I_{CC(B)}$                        |      |           |      |          |
|                    |                                       | $A\_EN = "0"$ ; $B\_EN = "0"$                  | -    | 3         | 5    | mA       |
|                    |                                       | $A\_EN = "1"$ ; $B\_EN = "1"$                  | -    | 245       | 280  | mA       |
| $G_p$              | power gain                            | maximum gain                                   | [1]  | 17.5      | 18.5 | 19.5 dB  |
|                    |                                       | minimum gain                                   | [2]  | -7        | -5.5 | -4 dB    |
| $R_{i(dif)}$       | differential input resistance         |                                                | 100  | 140       | 180  | $\Omega$ |
| $R_{o(dif)}$       | differential output resistance        |                                                | 160  | 200       | 240  | $\Omega$ |
| NF                 | noise figure                          | maximum gain                                   | [1]  | -         | 6    | 8 dB     |
|                    |                                       | increased rate per gain step                   | -    | 0.8       | 1    | dB       |
| $IP3_O$            | output third-order intercept point    | upper 5 gain steps                             | [1]  | -         | 43   | - dBm    |
| $P_{L(1dB)}$       | output power at 1 dB gain compression | upper 5 gain steps                             | [1]  | -         | 17   | - dBm    |
| $E_{G(dif)}$       | differential gain error               |                                                | -    | $\pm 0.1$ | -    | dB       |
| $E_{\varphi(dif)}$ | differential phase error              | upper 12 dB gain range                         | -    | 1.5       | -    | deg      |
|                    |                                       | per gain step (for all consecutive gain steps) | -    | 0.5       | -    | deg      |

[1] Maximum gain; gain code = 00000.

[2] Minimum gain; gain code = 11000.

## 2. Pinning information

### 2.1 Pinning

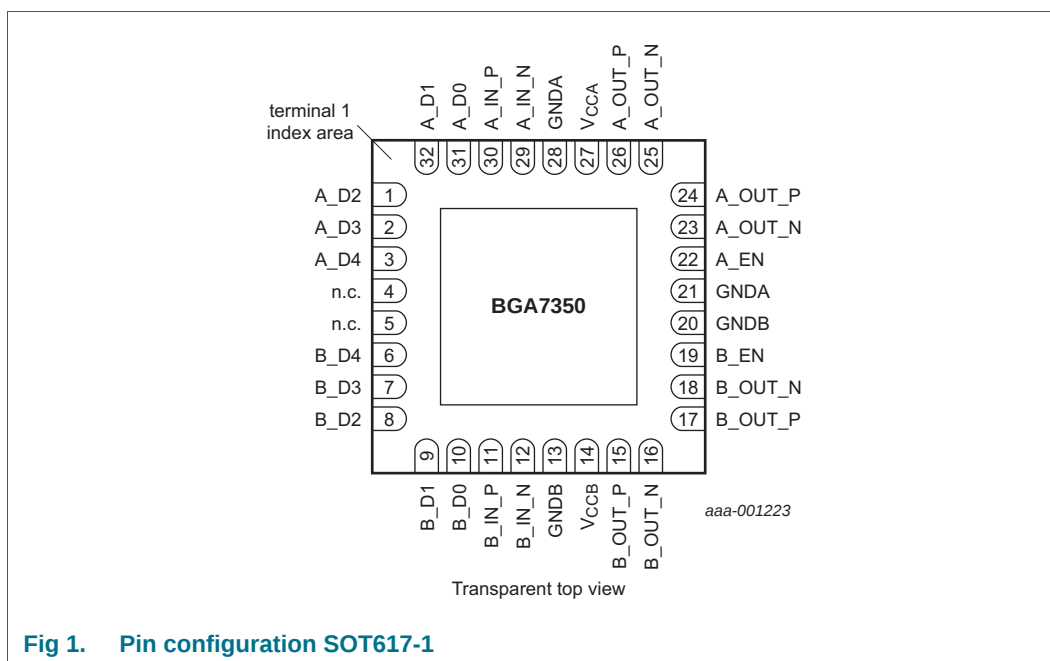


Fig 1. Pin configuration SOT617-1

### 2.2 Pin description

Table 2. Pin description

| Symbol           | Pin    | Description                                     |
|------------------|--------|-------------------------------------------------|
| A_D2             | 1      | MSB – 2 for gain control interface of channel A |
| A_D3             | 2      | MSB – 1 for gain control interface of channel A |
| A_D4             | 3      | MSB for gain control interface of channel A     |
| n.c.             | 4      | not connected <a href="#">[1]</a>               |
| n.c.             | 5      | not connected <a href="#">[1]</a>               |
| B_D4             | 6      | MSB for gain control interface of channel B     |
| B_D3             | 7      | MSB – 1 for gain control interface of channel B |
| B_D2             | 8      | MSB – 2 for gain control interface of channel B |
| B_D1             | 9      | LSB + 1 for gain control interface of channel B |
| B_D0             | 10     | LSB for gain control interface of channel B     |
| B_IN_P           | 11     | channel B positive input <a href="#">[2]</a>    |
| B_IN_N           | 12     | channel B negative input <a href="#">[2]</a>    |
| GNDB             | 13, 20 | ground for channel B                            |
| V <sub>CCB</sub> | 14     | supply voltage for channel B                    |
| B_OUT_P          | 15, 17 | channel B positive output <a href="#">[2]</a>   |
| B_OUT_N          | 16, 18 | channel B negative output <a href="#">[2]</a>   |
| B_EN             | 19     | power enable pin for channel B                  |
| GNDA             | 21, 28 | ground for channel A                            |

Table 2. Pin description ...continued

| Symbol           | Pin        | Description                                     |
|------------------|------------|-------------------------------------------------|
| A_EN             | 22         | power enable pin for channel A                  |
| A_OUT_N          | 23, 25     | channel A negative output [2]                   |
| A_OUT_P          | 24, 26     | channel A positive output [2]                   |
| V <sub>CCA</sub> | 27         | supply voltage for channel A                    |
| A_IN_N           | 29         | channel A negative input [2]                    |
| A_IN_P           | 30         | channel A positive input [2]                    |
| A_D0             | 31         | LSB for gain control interface of channel A     |
| A_D1             | 32         | LSB + 1 for gain control interface of channel A |
| GND              | GND paddle | RF ground and DC ground [3]                     |

[1] Pin to be left open.

[2] Each channel should be independently enabled with logic HIGH and disabled with logic LOW.

[3] The center metal base of the SOT617-1 also functions as heatsink for the VGA.

### 3. Ordering information

Table 3. Ordering information

| Type number | Package |                                                                                                    |          |
|-------------|---------|----------------------------------------------------------------------------------------------------|----------|
|             | Name    | Description                                                                                        | Version  |
| BGA7350     | HVQFN32 | plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 × 5 × 0.85 mm | SOT617-1 |

4. Functional diagram

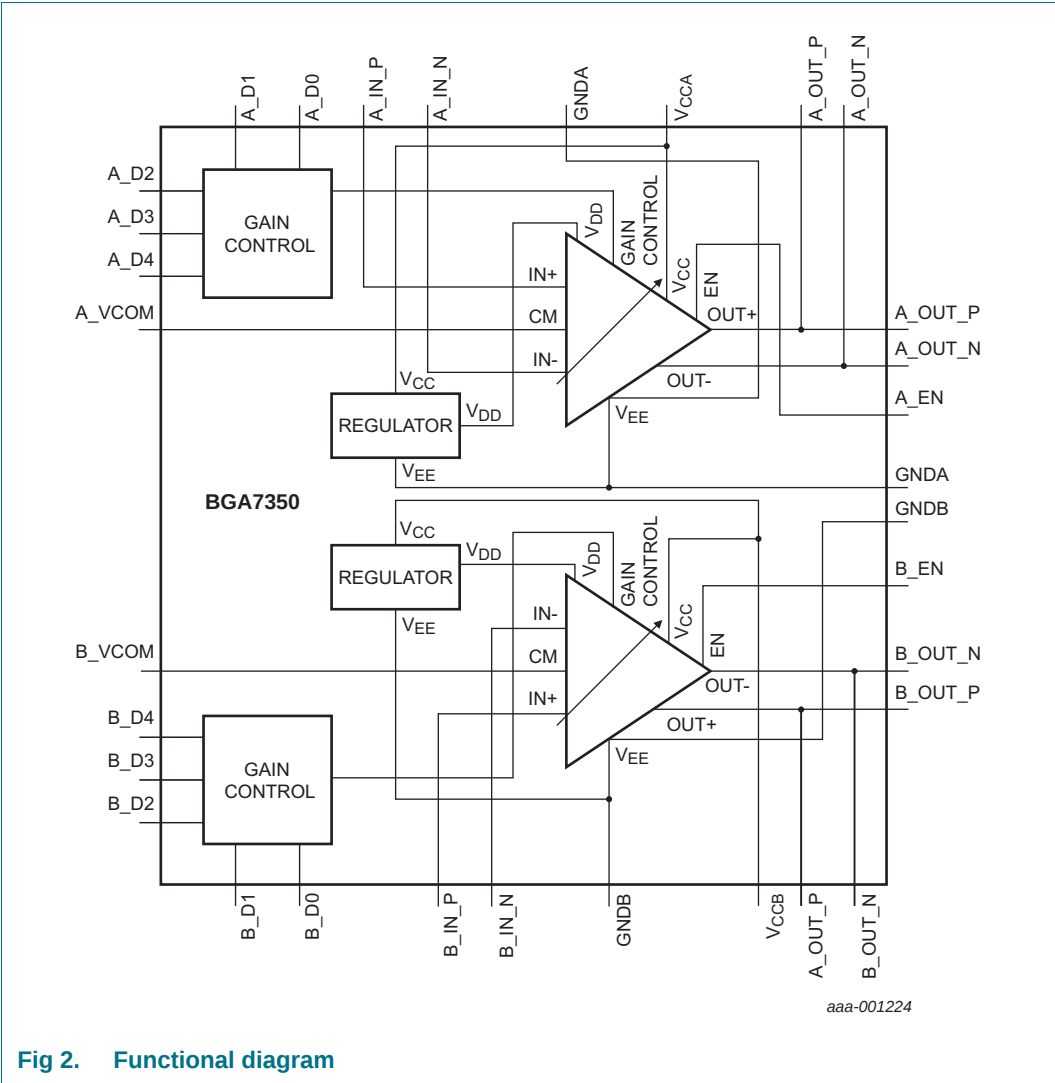


Fig 2. Functional diagram

5. Enable control

| Table 4. Enable / disable control settings |                       |                  |        |      |                     |      |                      |     |
|--------------------------------------------|-----------------------|------------------|--------|------|---------------------|------|----------------------|-----|
| Mode                                       | Function description  | Mode description | Enable |      | V <sub>EN</sub> (V) |      | I <sub>en</sub> (μA) |     |
|                                            |                       |                  | A_EN   | B_EN | Min                 | Max  | Min                  | Max |
| A_EN, B_EN                                 | VGA function off      | Disable          | "0"    | "0"  | 0                   | 0.8  | -                    | 1   |
| A_EN, B_EN                                 | VGA in operating mode | Enable           | "1"    | "1"  | 1.6                 | 5.25 | -                    | 1   |

## 6. Limiting values

**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol      | Parameter                       | Conditions                                                       | Min   | Max  | Unit |
|-------------|---------------------------------|------------------------------------------------------------------|-------|------|------|
| $V_{CC(A)}$ | supply voltage (A)              |                                                                  | [1] - | 6    | V    |
| $V_{CC(B)}$ | supply voltage (B)              |                                                                  | [1] - | 6    | V    |
| $V_{AEN}$   | voltage on pin A_EN             |                                                                  | -0.6  | 6    | V    |
| $V_{BEN}$   | voltage on pin B_EN             |                                                                  | -0.6  | 6    | V    |
| $V_{AD0}$   | voltage on pin A_D0             |                                                                  | -0.6  | 6    | V    |
| $V_{AD1}$   | voltage on pin A_D1             |                                                                  | -0.6  | 6    | V    |
| $V_{AD2}$   | voltage on pin A_D2             |                                                                  | -0.6  | 6    | V    |
| $V_{AD3}$   | voltage on pin A_D3             |                                                                  | -0.6  | 6    | V    |
| $V_{AD4}$   | voltage on pin A_D4             |                                                                  | -0.6  | 6    | V    |
| $V_{BD0}$   | voltage on pin B_D0             |                                                                  | -0.6  | 6    | V    |
| $V_{BD1}$   | voltage on pin B_D1             |                                                                  | -0.6  | 6    | V    |
| $V_{BD2}$   | voltage on pin B_D2             |                                                                  | -0.6  | 6    | V    |
| $V_{BD3}$   | voltage on pin B_D3             |                                                                  | -0.6  | 6    | V    |
| $V_{BD4}$   | voltage on pin B_D4             |                                                                  | -0.6  | 6    | V    |
| $V_{AIN}$   | voltage on pin A_IN             |                                                                  | -0.6  | 6    | V    |
| $V_{BIN}$   | voltage on pin B_IN             |                                                                  | -0.6  | 6    | V    |
| $P_{i(RF)}$ | RF input power                  |                                                                  | -     | 20   | dBm  |
| $T_{case}$  | case temperature                |                                                                  | -40   | +85  | °C   |
| $T_j$       | junction temperature            |                                                                  | -     | 150  | °C   |
| $V_{ESD}$   | electrostatic discharge voltage | Human Body Model (HBM);<br>According JEDEC standard 22-A114E     | -     | 4000 | V    |
|             |                                 | Charged Device Model (CDM);<br>According JEDEC standard 22-C101B | -     | 2000 | V    |
|             |                                 | Machine Model (MM);<br>According JEDEC standard 22-A115          | -     | 400  | V    |

[1] All digital pins may not exceed  $V_{CC}$  as the internal ESD circuit can be damaged. To prevent this it is recommended that  $V_{AEN}$  and  $V_{BEN}$  are limited to a maximum of 5 mA.

## 7. Thermal characteristics

**Table 6. Thermal characteristics**

| Symbol         | Parameter                                       | Conditions                                                                      | Typ | Unit |
|----------------|-------------------------------------------------|---------------------------------------------------------------------------------|-----|------|
| $R_{th(j-sp)}$ | thermal resistance from junction to solderpoint | $T_{case} = 85\text{ °C}$ ; $V_{CC} = 5\text{ V}$ ;<br>$I_{CC} = 245\text{ mA}$ | 17  | K/W  |

## 8. Static characteristics

**Table 7. Characteristics**

$A\_EN = "1"$ ;  $B\_EN = "1"$  (both channels enabled). Typical values at  $V_{CC} = 5\text{ V}$ ;  $T_{case} = 25\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

| Symbol   | Parameter                | Conditions                    | Min  | Typ | Max  | Unit |
|----------|--------------------------|-------------------------------|------|-----|------|------|
| $V_{CC}$ | supply voltage           | $V_{CC(A)} + V_{CC(B)}$       | 4.75 | 5   | 5.25 | V    |
| $I_{CC}$ | supply current           | $I_{CC(A)} + I_{CC(B)}$       |      |     |      |      |
|          |                          | $A\_EN = "0"$ ; $B\_EN = "0"$ | -    | 3   | 5    | mA   |
|          |                          | $A\_EN = "1"$ ; $B\_EN = "1"$ | -    | 245 | 280  | mA   |
| $V_{IH}$ | HIGH-level input voltage | [1]                           | 1.6  | -   | 5.25 | V    |
| $V_{IL}$ | LOW-level input voltage  | [1]                           | -    | -   | 0.8  | V    |
| $P_L$    | power dissipation        |                               | -    | 1.2 | 1.5  | W    |

[1] Voltage on the control pins.

## 9. Dynamic characteristics

**Table 8. Characteristics**

$A\_EN = "1"$ ;  $B\_EN = "1"$  (VGA enabled). Typical values at  $V_{CC} = 5\text{ V}$ ;  $I_{CC} = 245\text{ mA}$ ; Tuned for  $f_{IF} = 172\text{ MHz}$ ;  $B = 28\text{ MHz}$ ;  $T_{case} = 25\text{ }^{\circ}\text{C}$ ; Differential input resistance matched to  $140\text{ }\Omega$ ; Differential output resistance matched to  $200\text{ }\Omega$ ; unless otherwise specified; see [Section 11 "Application information"](#).

| Symbol           | Parameter                | Conditions                                     | Min  | Typ       | Max  | Unit          |
|------------------|--------------------------|------------------------------------------------|------|-----------|------|---------------|
| $G_p$            | power gain               | maximum gain                                   | [1]  |           |      |               |
|                  |                          | $f = 50\text{ MHz}$ ; $B = 15\text{ MHz}$      | -    | 19.5      | -    | dB            |
|                  |                          | $f = 172\text{ MHz}$ ; $B = 28\text{ MHz}$     | 17.5 | 18.5      | 19.5 | dB            |
|                  |                          | $f = 250\text{ MHz}$ ; $B = 28\text{ MHz}$     | -    | 18.0      | -    | dB            |
|                  |                          | minimum gain                                   | [2]  |           |      |               |
|                  |                          | $f = 50\text{ MHz}$ ; $B = 15\text{ MHz}$      | -    | -4.5      | -    | dB            |
|                  |                          | $f = 172\text{ MHz}$ ; $B = 28\text{ MHz}$     | -7   | -5.5      | -4   | dB            |
|                  |                          | $f = 250\text{ MHz}$ ; $B = 28\text{ MHz}$     | -    | -6.0      | -    | dB            |
| $\Delta G_{adj}$ | gain adjustment range    | [1]                                            | -    | 24        | -    | dB            |
| $G_{step}$       | gain step                |                                                | -    | 1         | -    |               |
| $G_{flat}$       | gain flatness            | [1]                                            | -    | 0.1       | -    | dB            |
| $E_{G(dif)}$     | differential gain error  |                                                | -    | $\pm 0.1$ | -    | dB            |
| $E_{G(itg)}$     | integrated gain error    | upper 12 dB gain range                         | -    | $\pm 0.3$ | -    | dB            |
|                  |                          | full gain range                                | -    | $\pm 0.4$ | -    | dB            |
| $E_{\phi(dif)}$  | differential phase error | upper 12 dB gain range                         | -    | 1.5       | -    | deg           |
|                  |                          | per gain step (for all consecutive gain steps) | -    | 0.5       | -    | deg           |
| $t_{s(step)G}$   | gain step settling time  | per 1.5 dB of steady state                     | -    | 5         | 15   | ns            |
|                  |                          | per 0.1 dB of steady state                     | -    | 20        | 40   | ns            |
| $t_{d(grp)}$     | group delay time         |                                                | -    | 150       | -    | ps            |
| $t_{pu}$         | power-up time            |                                                | -    | -         | 1    | $\mu\text{s}$ |

**Table 8. Characteristics ...continued**

$A\_EN = "1"$ ;  $B\_EN = "1"$  (VGA enabled). Typical values at  $V_{CC} = 5\text{ V}$ ;  $I_{CC} = 245\text{ mA}$ ; Tuned for  $f_{IF} = 172\text{ MHz}$ ;  $B = 28\text{ MHz}$ ;  $T_{case} = 25\text{ }^{\circ}\text{C}$ ; Differential input resistance matched to  $140\text{ }\Omega$ ; Differential output resistance matched to  $200\text{ }\Omega$ ; unless otherwise specified; see [Section 11](#) "Application information".

| Symbol                 | Parameter                             | Conditions                  | Min     | Typ | Max | Unit     |
|------------------------|---------------------------------------|-----------------------------|---------|-----|-----|----------|
| $R_{i(dif)}$           | differential input resistance         |                             | 100     | 140 | 180 | $\Omega$ |
| $R_{o(dif)}$           | differential output resistance        |                             | 160     | 200 | 240 | $\Omega$ |
| $\alpha_{isol(ch-ch)}$ | isolation between channels            |                             | 50      | -   | -   | dB       |
| CMRR                   | common-mode rejection ratio           |                             | 40      | -   | -   | dB       |
| IP3 <sub>O</sub>       | output third-order intercept point    | Upper 5 gain steps          | [3]     |     |     |          |
|                        |                                       | f = 50 MHz                  | [4]     | -   | 43  | - dBm    |
|                        |                                       | f = 172 MHz                 | [5]     | -   | 43  | - dBm    |
|                        |                                       | f = 250 MHz                 | [6]     | -   | 41  | - dBm    |
| IP2 <sub>O</sub>       | output second-order intercept point   | Upper 5 gain steps          | [3]     |     |     |          |
|                        |                                       | f = 50 MHz                  | [7]     | -   | 85  | - dBm    |
|                        |                                       | f = 172 MHz                 | [8]     | -   | 70  | - dBm    |
|                        |                                       | f = 250 MHz                 | [9]     | -   | 70  | - dBm    |
| P <sub>L(1dB)</sub>    | output power at 1 dB gain compression | Upper 5 gain steps          | [3]     |     |     |          |
|                        |                                       | f = 50 MHz                  | -       | 17  | -   | - dBm    |
|                        |                                       | f = 172 MHz                 | -       | 17  | -   | - dBm    |
|                        |                                       | f = 250 MHz                 | -       | 17  | -   | - dBm    |
| $\alpha_{2H}$          | second harmonic level                 | maximum gain                | [1][10] | -   | -80 | - dBc    |
|                        |                                       | gain step 12                | [2][10] | -   | -80 | - dBc    |
| NF                     | noise figure                          | maximum gain                | [1]     | -   | 6   | 8 dB     |
|                        |                                       | increase rate per gain step | -       | 0.8 | 1   | dB       |

[1] Maximum gain; gain code = 00000.

[2] Minimum gain; gain code = 11000.

[3] Gain code = 00000, 00001, 00010, 00011, 00100.

[4]  $P_L = 2\text{ dBm}$  per tone; spacing = 2 MHz ( $f_1 = 49\text{ MHz}$ ;  $f_2 = 51\text{ MHz}$ )

[5]  $P_L = 2\text{ dBm}$  per tone; spacing = 2 MHz ( $f_1 = 171\text{ MHz}$ ;  $f_2 = 173\text{ MHz}$ )

[6]  $P_L = 2\text{ dBm}$  per tone; spacing = 2 MHz ( $f_1 = 249\text{ MHz}$ ;  $f_2 = 251\text{ MHz}$ )

[7]  $P_L = 2\text{ dBm}$  per tone ( $f_1 = 30\text{ MHz}$ ;  $f_2 = 80\text{ MHz}$ ;  $f_{meas} = 50\text{ MHz}$ )

[8]  $P_L = 2\text{ dBm}$  per tone ( $f_1 = 82\text{ MHz}$ ;  $f_2 = 90\text{ MHz}$ ;  $f_{meas} = 172\text{ MHz}$ )

[9]  $P_L = 2\text{ dBm}$  per tone ( $f_1 = 120\text{ MHz}$ ;  $f_2 = 130\text{ MHz}$ ;  $f_{meas} = 250\text{ MHz}$ )

[10]  $P_L = 5\text{ dBm}$  one tone ( $f = 86\text{ MHz}$ ;  $f_{meas} = 172\text{ MHz}$ )

Table 9. Gain control

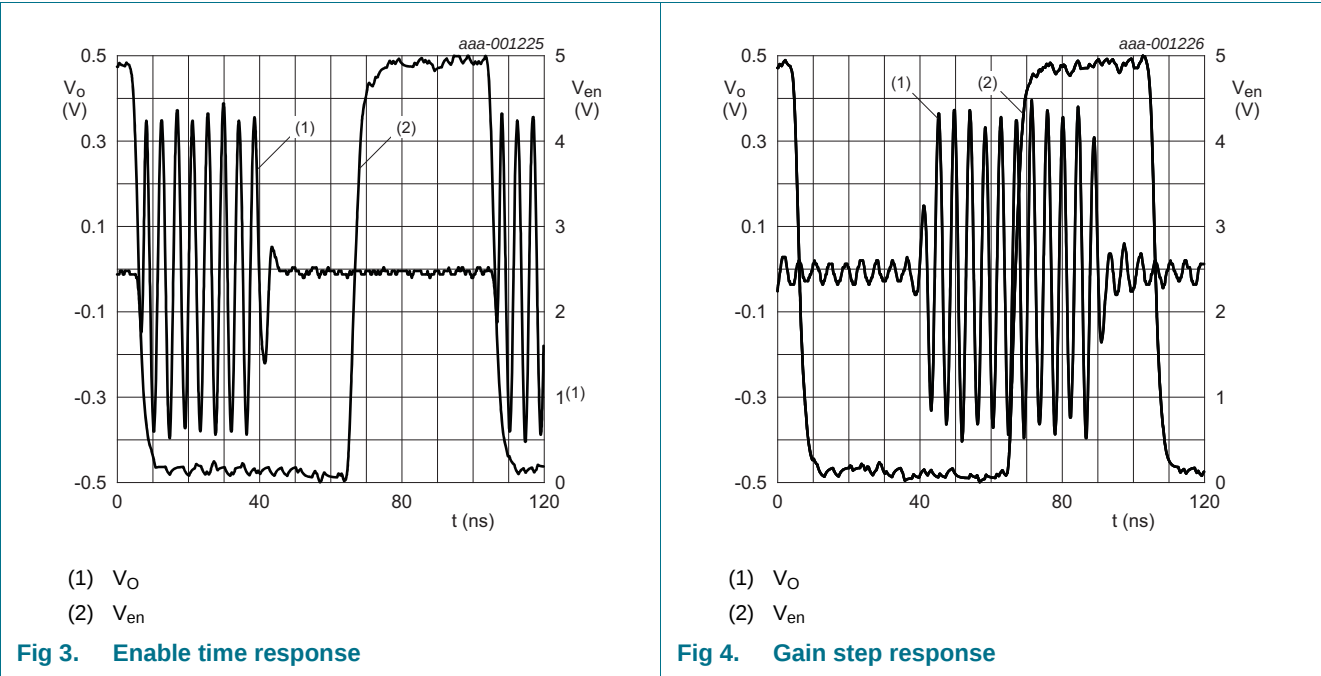
| gain step | input to either A_D0 to A_D4 pins<br>or B_D0 to B_D4 pins | nominal power gain (dB) |
|-----------|-----------------------------------------------------------|-------------------------|
| 0         | 00000                                                     | 18.5                    |
| 1         | 00001                                                     | 17.5                    |
| 2         | 00010                                                     | 16.5                    |
| 3         | 00011                                                     | 15.5                    |
| 4         | 00100                                                     | 14.5                    |
| 5         | 00101                                                     | 13.5                    |
| 6         | 00110                                                     | 12.5                    |
| 7         | 00111                                                     | 11.5                    |
| 8         | 01000                                                     | 10.5                    |
| 9         | 01001                                                     | 9.5                     |
| 10        | 01010                                                     | 8.5                     |
| 11        | 01011                                                     | 7.5                     |
| 12        | 01100                                                     | 6.5                     |
| 13        | 01101                                                     | 5.5                     |
| 14        | 01110                                                     | 4.5                     |
| 15        | 01111                                                     | 3.5                     |
| 16        | 10000                                                     | 2.5                     |
| 17        | 10001                                                     | 1.5                     |
| 18        | 10010                                                     | 0.5                     |
| 19        | 10011                                                     | -0.5                    |
| 20        | 10100                                                     | -1.5                    |
| 21        | 10101                                                     | -2.5                    |
| 22        | 10110                                                     | -3.5                    |
| 23        | 10111                                                     | -4.5                    |
| 24        | 11000                                                     | -5.5                    |
| -         | > 11000                                                   | -5.5                    |

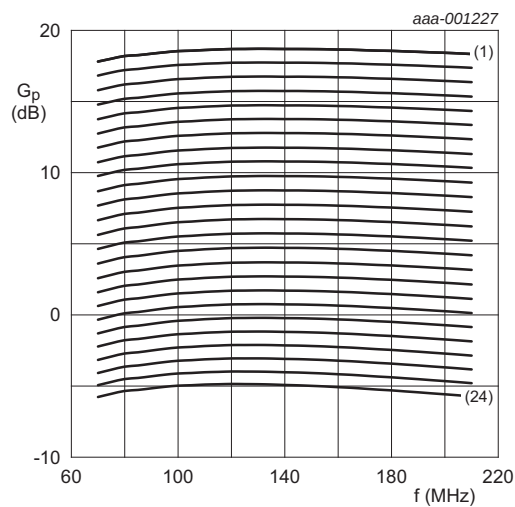
## 10. Moisture sensitivity

Table 10. Moisture sensitivity level

| Test methodology | Class |
|------------------|-------|
| JESD-22-A113     | 2     |

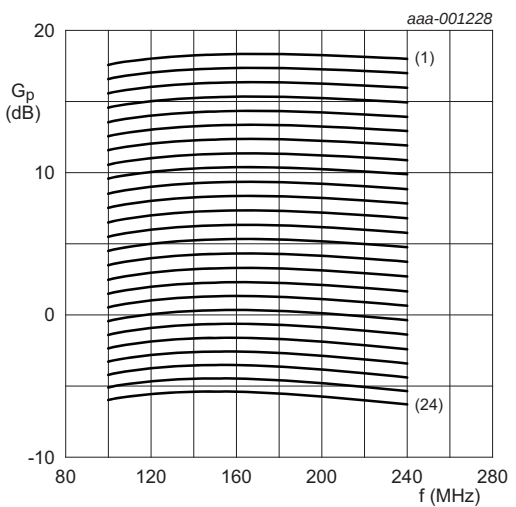
11. Application information





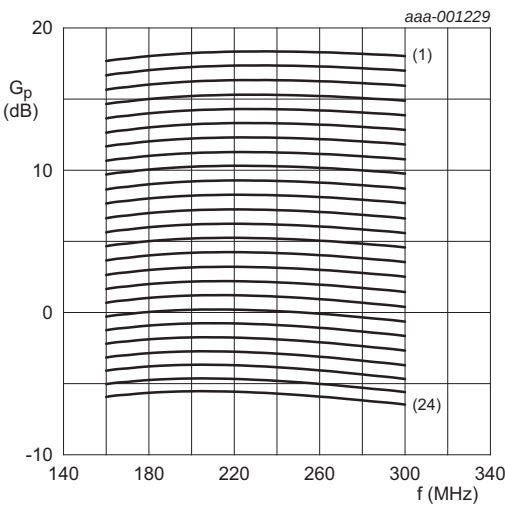
Tuned for  $f_{IF} = 140$  MHz;  $P_L = 5$  dBm; step size 1 dB.  
(1) gain step 0 (maximum gain)  
(25) gain step 24 (minimum gain)

Fig 5. Power gain as a function of frequency



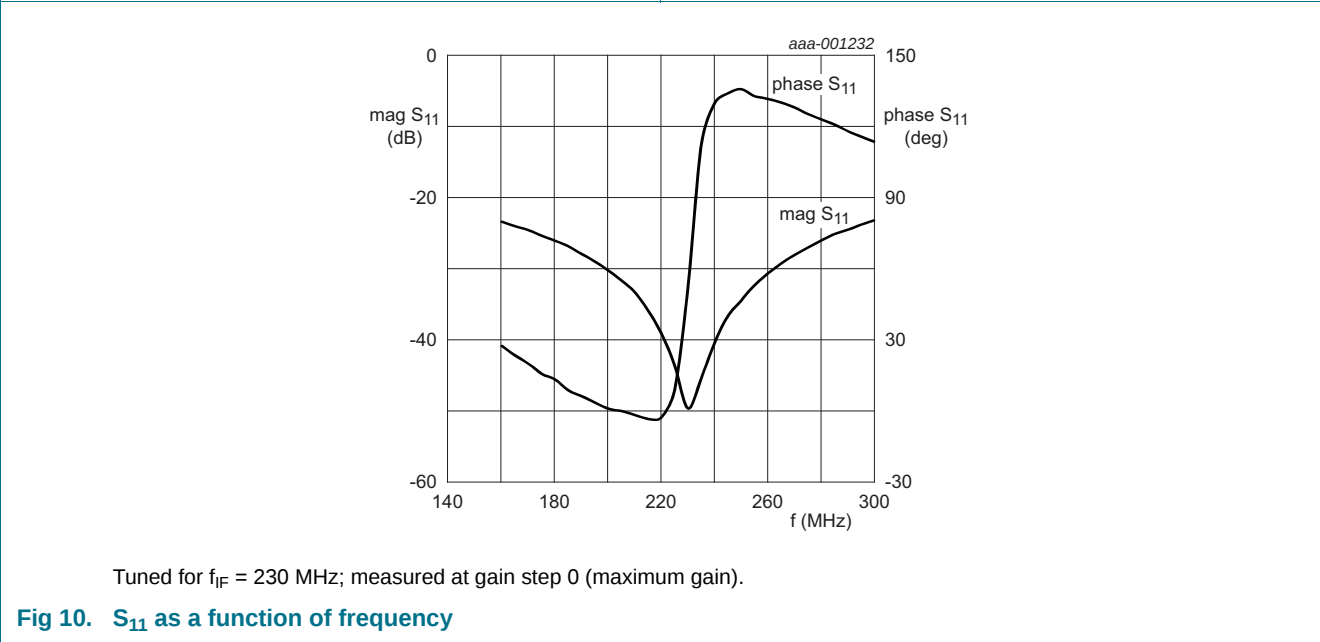
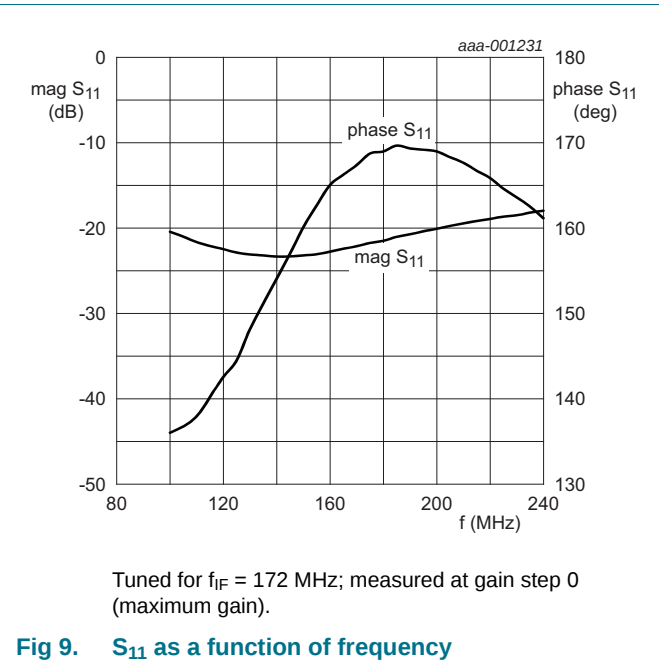
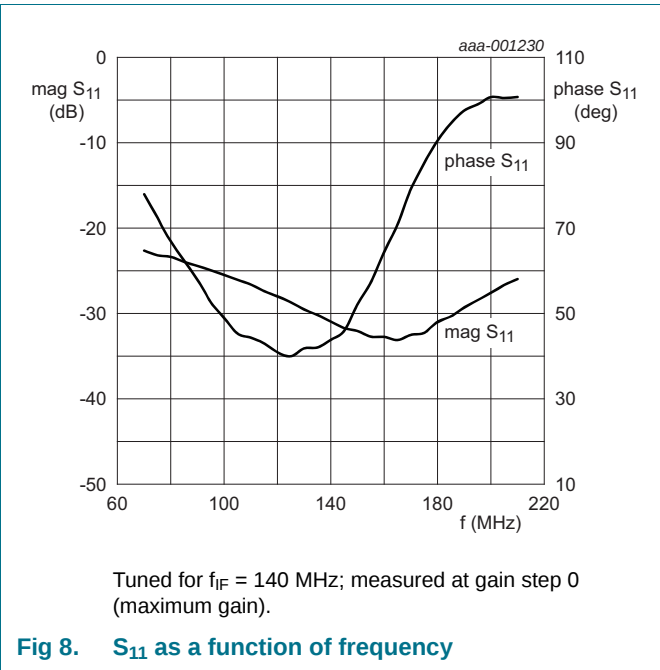
Tuned for  $f_{IF} = 172$  MHz;  $P_L = 5$  dBm; step size 1 dB.  
(1) gain step 0 (maximum gain)  
(25) gain step 24 (minimum gain)

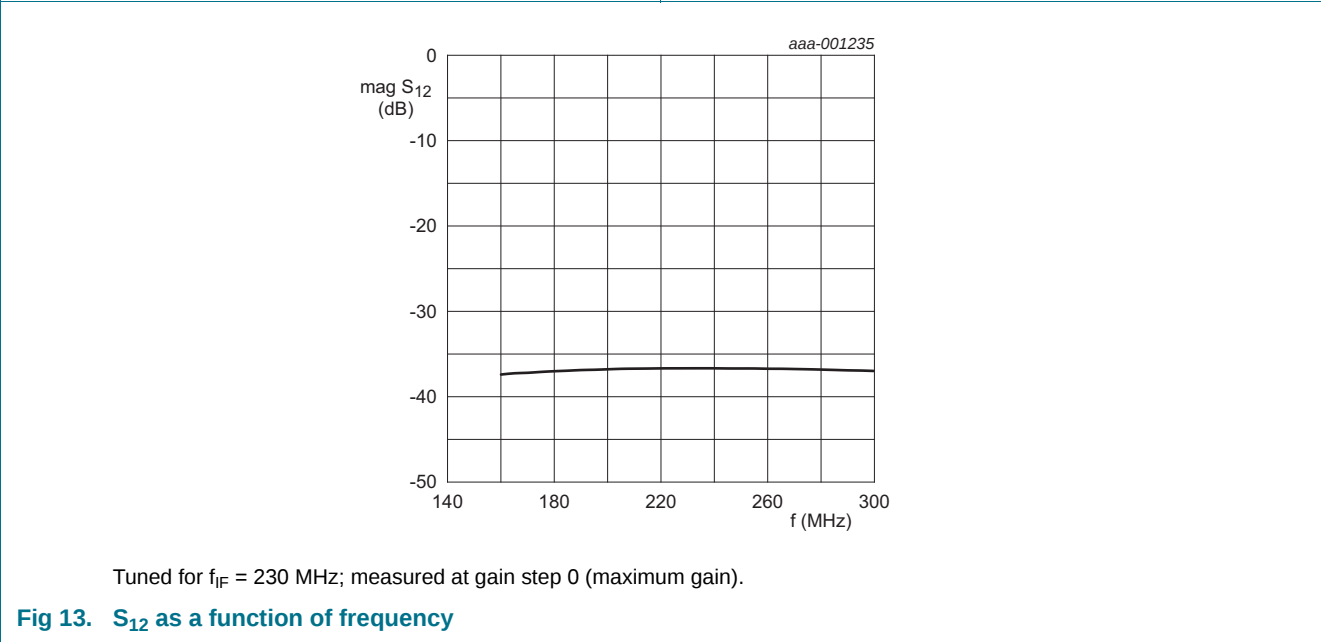
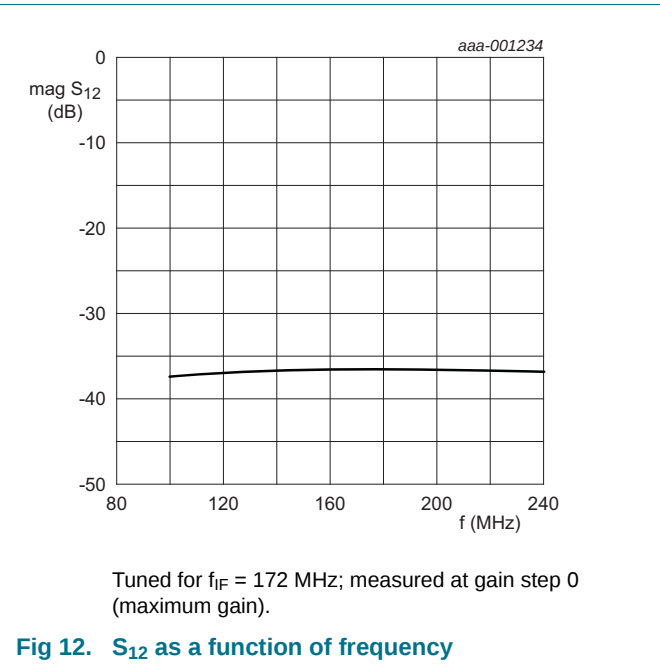
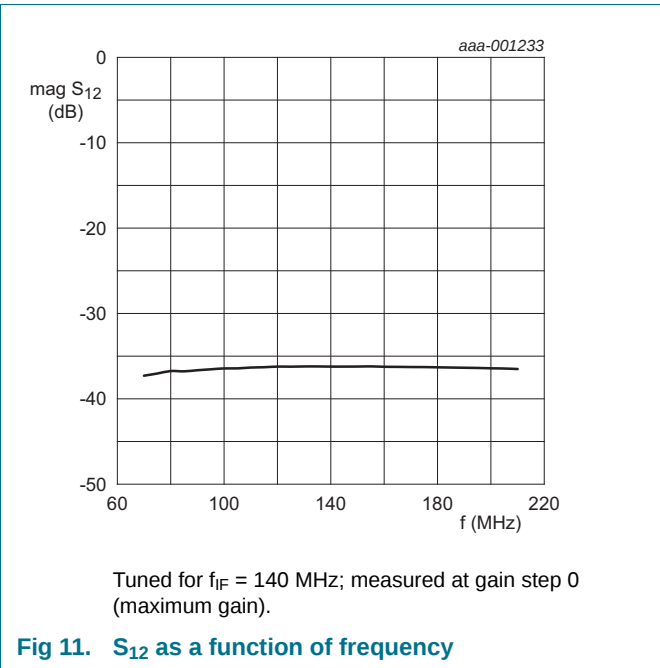
Fig 6. Power gain as a function of frequency

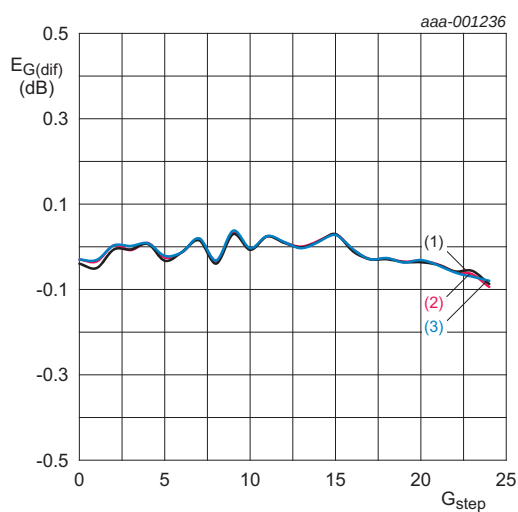


Tuned for  $f_{IF} = 230$  MHz;  $P_L = 5$  dBm; step size 1 dB.  
(1) gain step 0 (maximum gain)  
(25) gain step 24 (minimum gain)

Fig 7. Power gain as a function of frequency



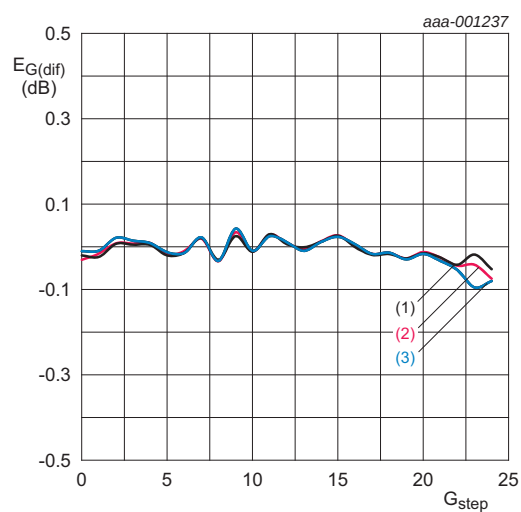




Tuned for  $f_{IF} = 140$  MHz.

- (1)  $T_{amb} = -40$  °C
- (2)  $T_{amb} = +25$  °C
- (3)  $T_{amb} = +85$  °C

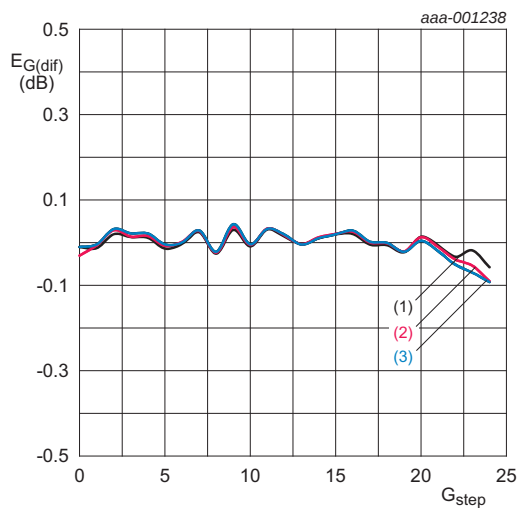
**Fig 14. Differential gain error as a function of gain step**



Tuned for  $f_{IF} = 172$  MHz.

- (1)  $T_{amb} = -40$  °C
- (2)  $T_{amb} = +25$  °C
- (3)  $T_{amb} = +85$  °C

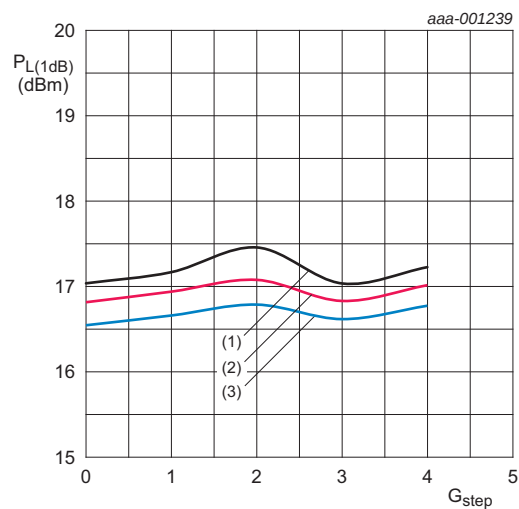
**Fig 15. Differential gain error as a function of gain step**



Tuned for  $f_{IF} = 230$  MHz.

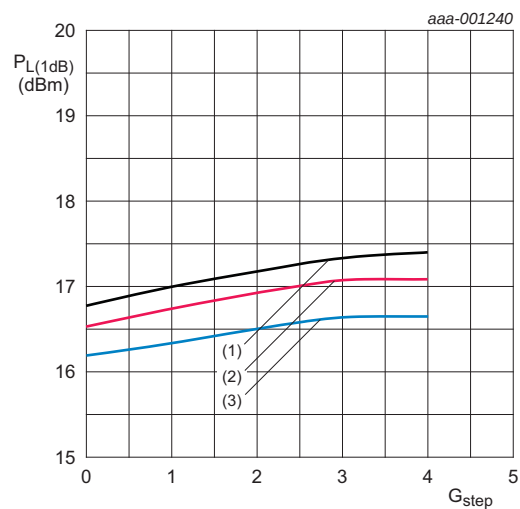
- (1)  $T_{amb} = -40$  °C
- (2)  $T_{amb} = +25$  °C
- (3)  $T_{amb} = +85$  °C

**Fig 16. Differential gain error as a function of gain step**



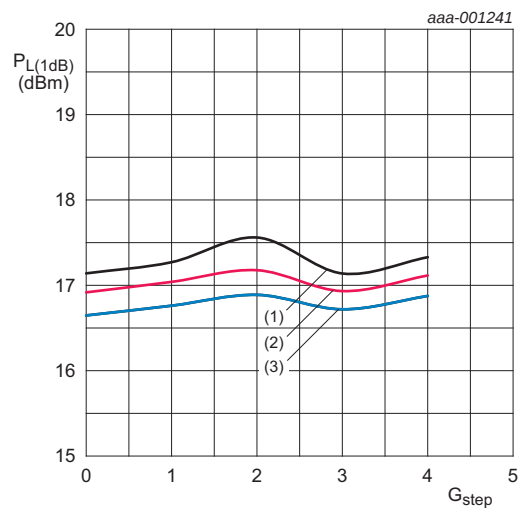
Tuned for  $f_{IF} = 140$  MHz.  
(1)  $T_{amb} = -40$  °C  
(2)  $T_{amb} = +25$  °C  
(3)  $T_{amb} = +85$  °C

Fig 17. output power at 1 dB gain compression as a function of gain step



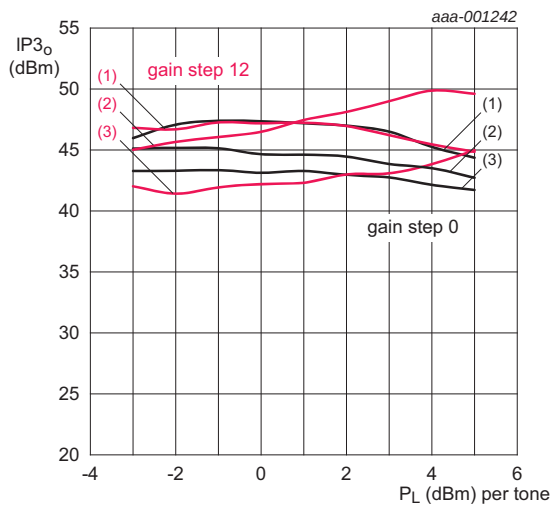
Tuned for  $f_{IF} = 172$  MHz.  
(1)  $T_{amb} = -40$  °C  
(2)  $T_{amb} = +25$  °C  
(3)  $T_{amb} = +85$  °C

Fig 18. output power at 1 dB gain compression as a function of gain step



Tuned for  $f_{IF} = 230$  MHz.  
(1)  $T_{amb} = -40$  °C  
(2)  $T_{amb} = +25$  °C  
(3)  $T_{amb} = +85$  °C

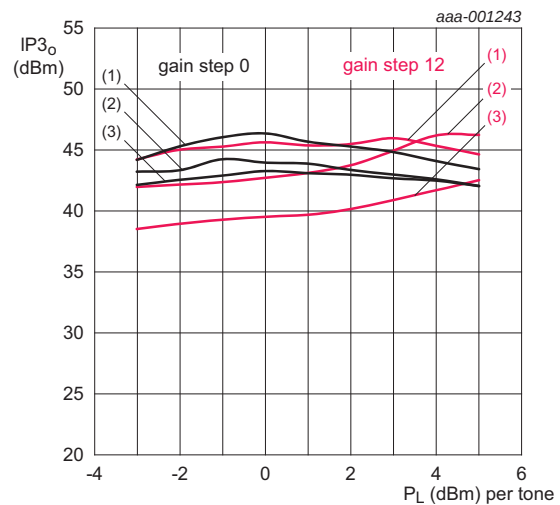
Fig 19. output power at 1 dB gain compression as a function of gain step



Tuned for  $f_{IF} = 140$  MHz.

- (1)  $T_{amb} = -40$  °C
- (2)  $T_{amb} = +25$  °C
- (3)  $T_{amb} = +85$  °C

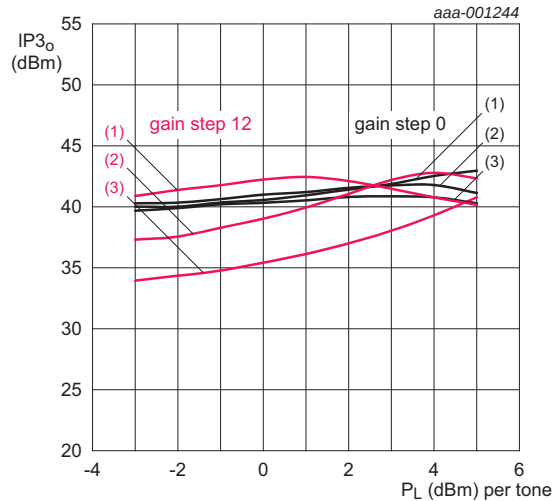
**Fig 20. Output third order intercept point as a function of output power per tone**



Tuned for  $f_{IF} = 172$  MHz.

- (1)  $T_{amb} = -40$  °C
- (2)  $T_{amb} = +25$  °C
- (3)  $T_{amb} = +85$  °C

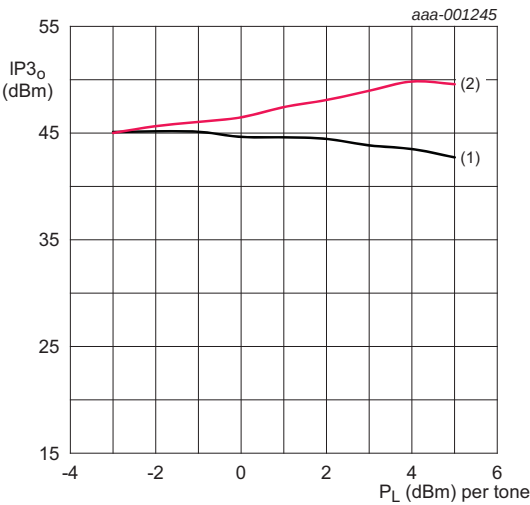
**Fig 21. Output third order intercept point as a function of output power per tone**



Tuned for  $f_{IF} = 230$  MHz.

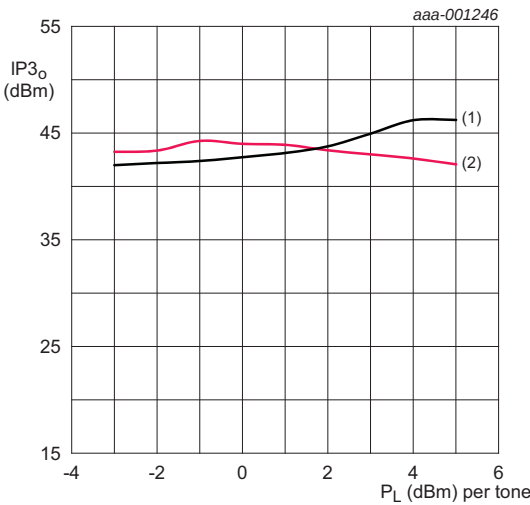
- (1)  $T_{amb} = -40$  °C
- (2)  $T_{amb} = +25$  °C
- (3)  $T_{amb} = +85$  °C

**Fig 22. Output third order intercept point as a function of output power per tone**



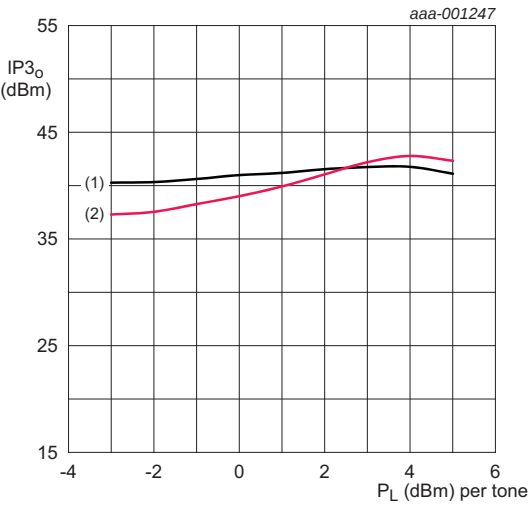
Tuned for  $f_{IF} = 140$  MHz.  
(1) gain step 0  
(2) gain step 12

Fig 23. Output third order intercept point as a function of output power per tone



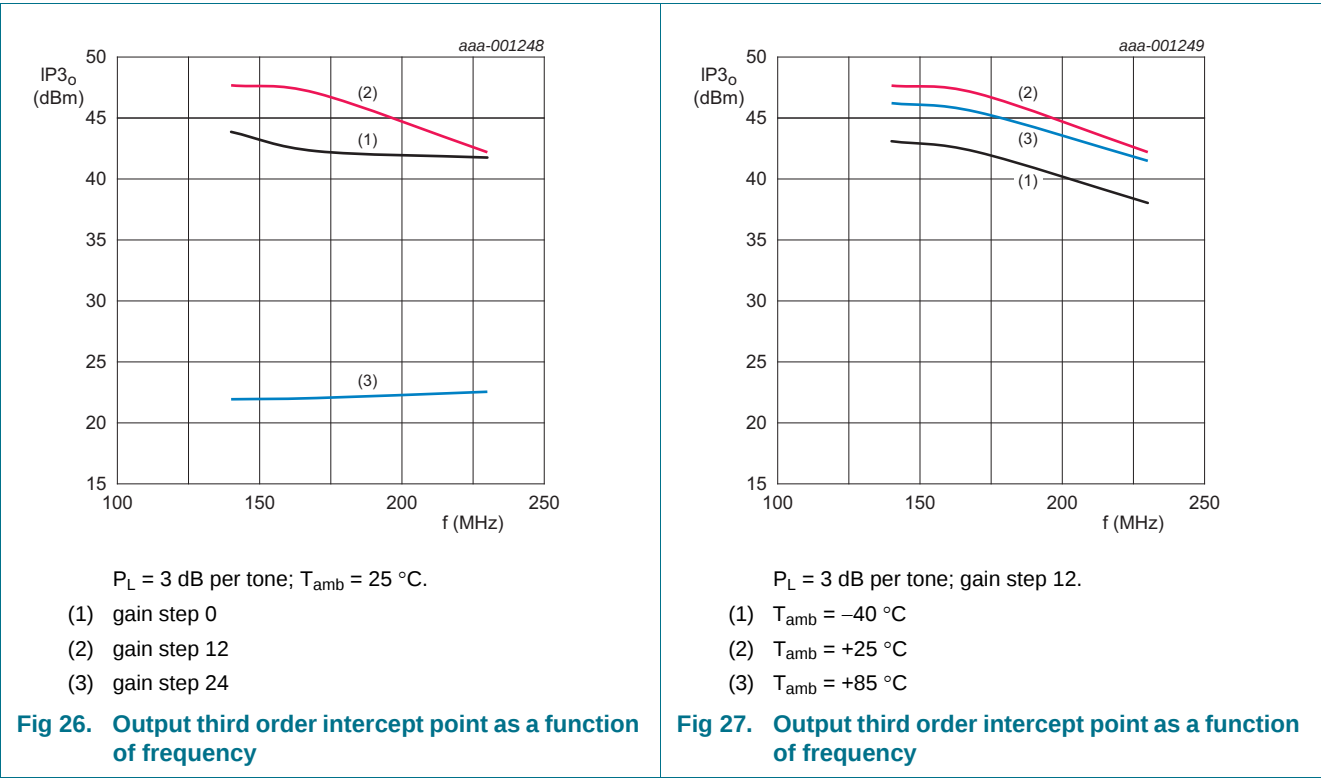
Tuned for  $f_{IF} = 172$  MHz.  
(1) gain step 0  
(2) gain step 12

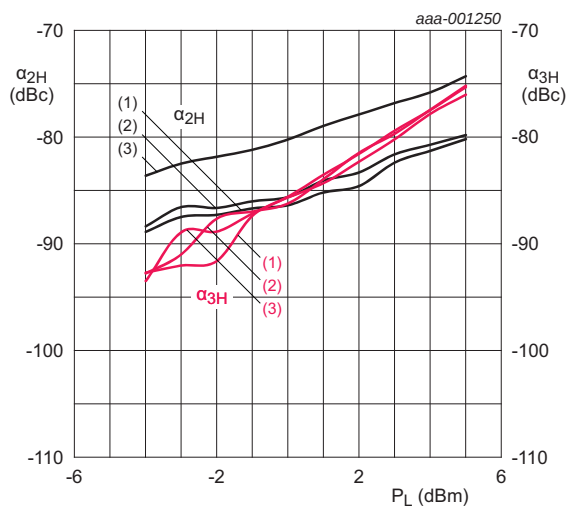
Fig 24. Output third order intercept point as a function of output power per tone



Tuned for  $f_{IF} = 230$  MHz.  
(1) gain step 0  
(2) gain step 12

Fig 25. Output third order intercept point as a function of output power per tone

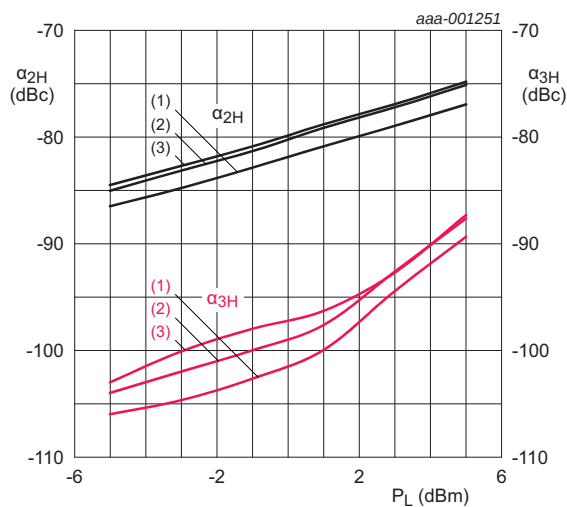




Tuned for  $f_{IF} = 86$  MHz;  $f_{2H} = 172$  MHz;  $f_{3H} = 258$  MHz; gain step 0 (maximum gain).

- (1)  $T_{amb} = -40$  °C
- (2)  $T_{amb} = +25$  °C
- (3)  $T_{amb} = +85$  °C

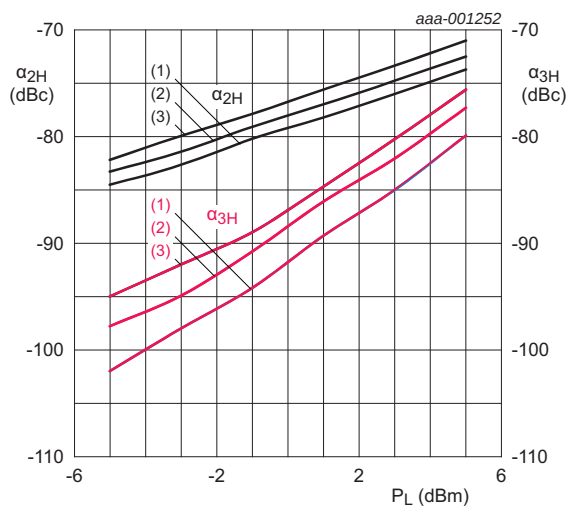
**Fig 28. Second harmonic level and third harmonic level as a function of output power**



Tuned for  $f_{IF} = 140$  MHz;  $f_{2H} = 280$  MHz;  $f_{3H} = 420$  MHz; gain step 0 (maximum gain).

- (1)  $T_{amb} = -40$  °C
- (2)  $T_{amb} = +25$  °C
- (3)  $T_{amb} = +85$  °C

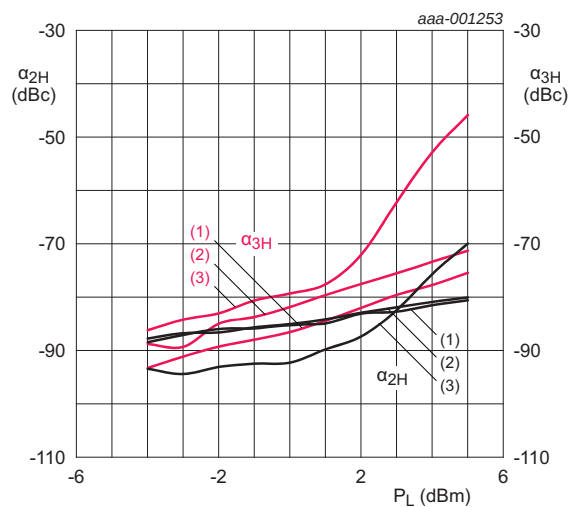
**Fig 29. Second harmonic level and third harmonic level as a function of output power**



Tuned for  $f_{IF} = 230$  MHz;  $f_{2H} = 460$  MHz;  $f_{3H} = 690$  MHz; gain step 0 (maximum gain).

- (1)  $T_{amb} = -40$  °C
- (2)  $T_{amb} = +25$  °C
- (3)  $T_{amb} = +85$  °C

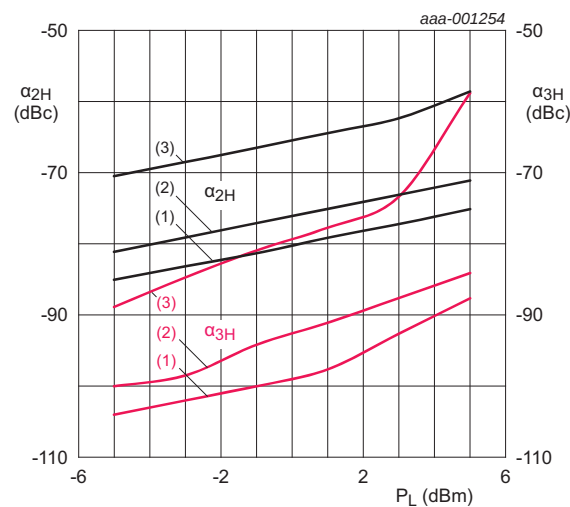
**Fig 30. Second harmonic level and third harmonic level as a function of output power**



Tuned for  $f_{IF} = 86$  MHz;  $f_{2H} = 172$  MHz;  $f_{3H} = 358$  MHz;  $T_{amb} = 25$  °C.

(1) gain step 0  
(2) gain step 12  
(3) gain step 24

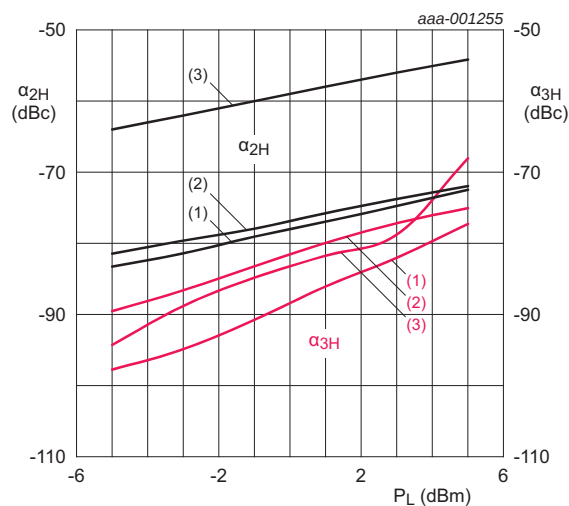
Fig 31. Second harmonic level and third harmonic level as a function of output power



Tuned for  $f_{IF} = 140$  MHz;  $f_{2H} = 280$  MHz;  $f_{3H} = 420$  MHz;  $T_{amb} = 25$  °C.

(1) gain step 0  
(2) gain step 12  
(3) gain step 24

Fig 32. Second harmonic level and third harmonic level as a function of output power

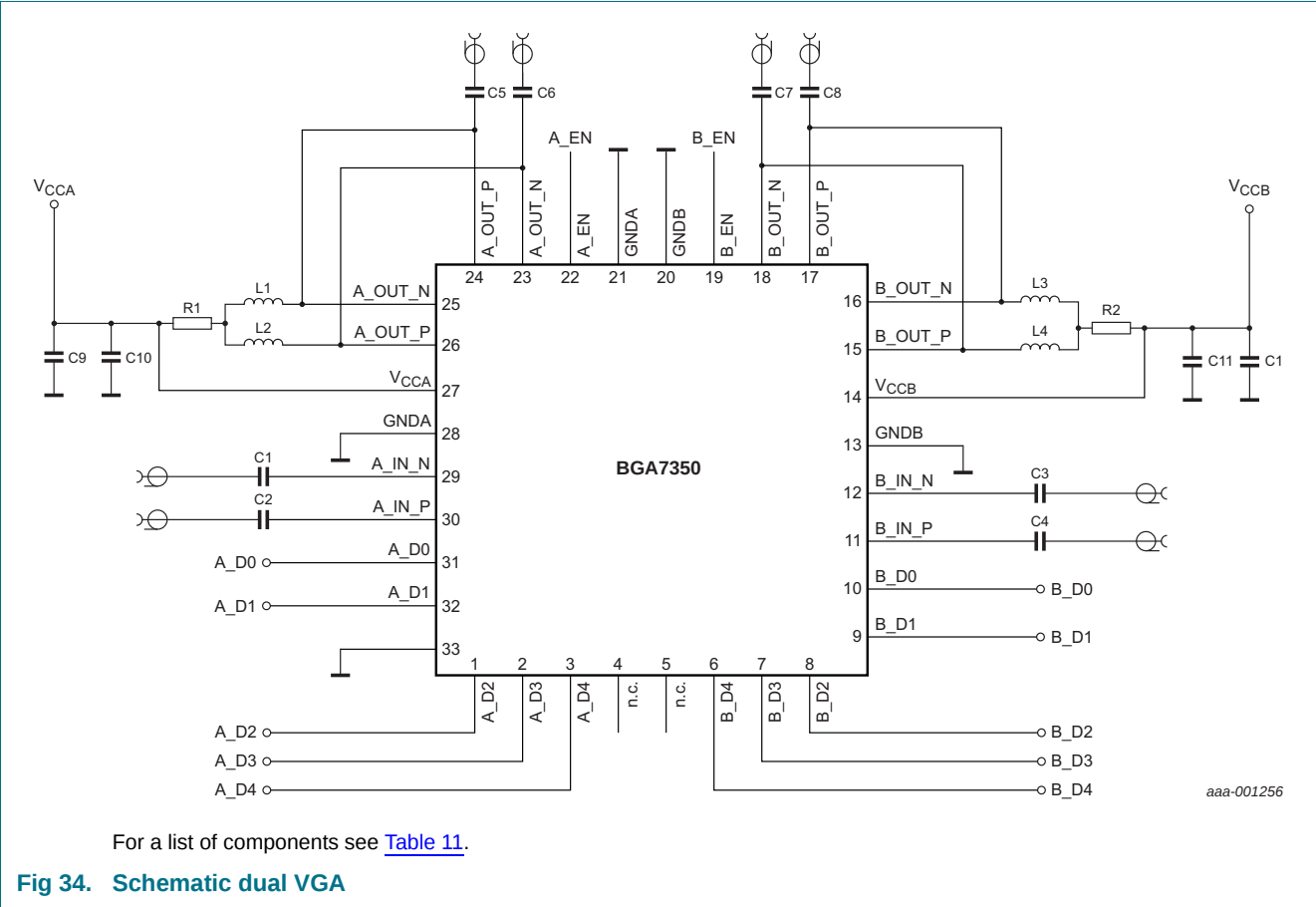


Tuned for  $f_{IF} = 230$  MHz;  $f_{2H} = 460$  MHz;  $f_{3H} = 690$  MHz;  $T_{amb} = 25$  °C.

(1) gain step 0  
(2) gain step 12  
(3) gain step 24

Fig 33. Second harmonic level and third harmonic level as a function of output power

11.1 Schematic dual VGA



For a list of components see [Table 11](#).

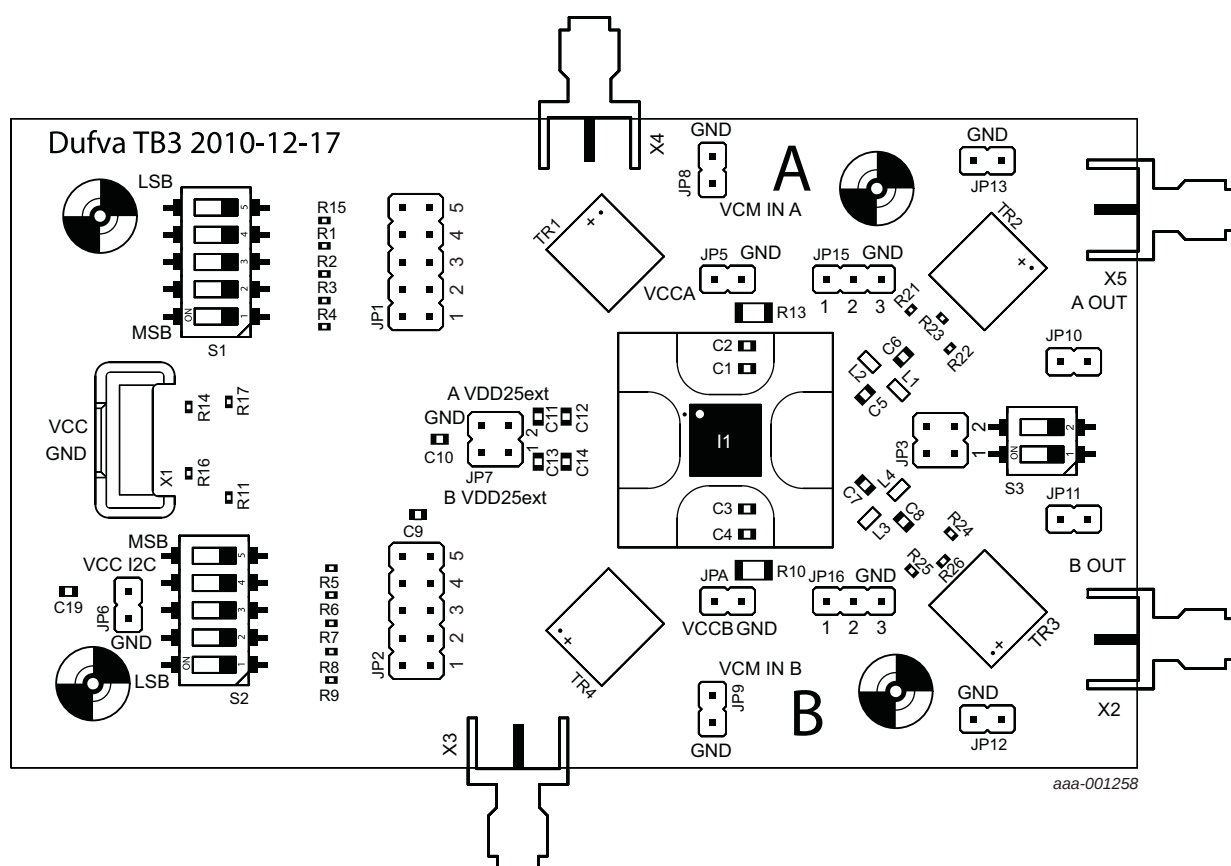
Fig 34. Schematic dual VGA

Table 11. List of components  
For schematic see [Figure 34](#).

| Component                               | Description | Conditions  | Value   | Remarks |
|-----------------------------------------|-------------|-------------|---------|---------|
| C1, C2, C3, C4, C5, C6, C7, C8, C9, C11 | capacitor   |             | 1 nF    |         |
| C10, C12                                | capacitor   |             | 100 pF  |         |
| L1, L2, L3, L4                          | inductor    | f = 50 MHz  | 1200 nH | 0603LS  |
|                                         |             | f = 172 MHz | 120 nH  | 0603LS  |
|                                         |             | f = 250 MHz | 56 nH   | 0603LS  |
| R1, R2                                  | resistor    |             | 0 Ω     |         |

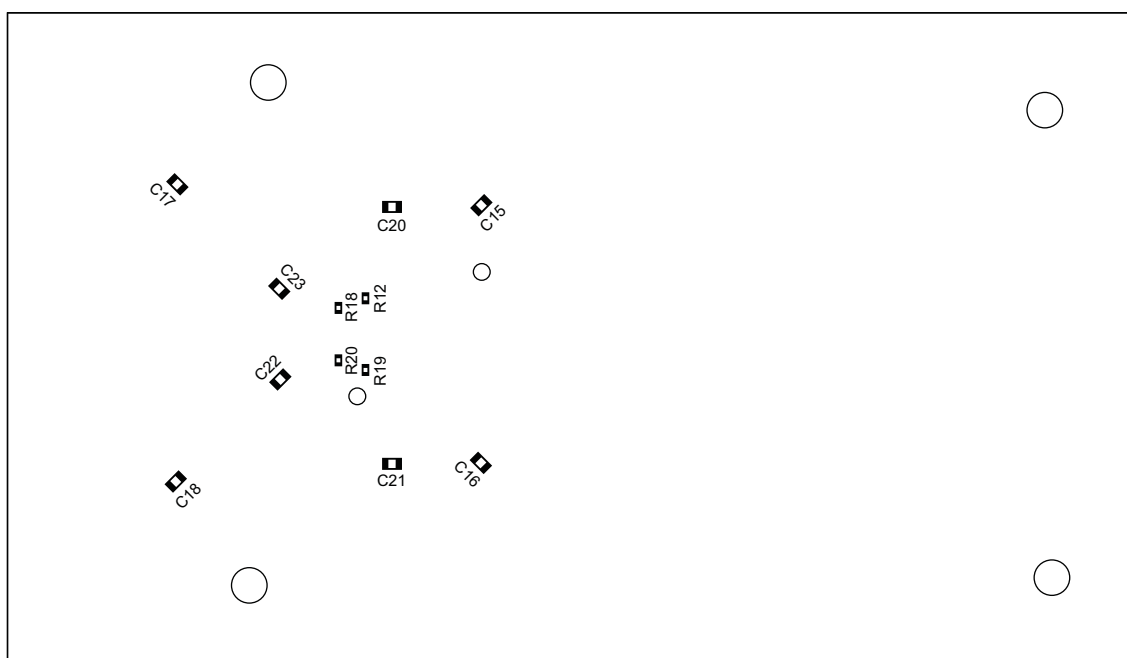


**Fig 35. Schematic**



For a list of components see [Table 12](#).

**Fig 36. Components top side**



aaa-001259

For a list of components see [Table 12](#).

**Fig 37. Components bottom side**

**Table 12. List of components**

See [Figure 35](#), [Figure 36](#) and [Figure 37](#).

| Component               | Description | Conditions | Value     | Size | Remarks     |
|-------------------------|-------------|------------|-----------|------|-------------|
| C1, C3, C6, C8, C9      | capacitor   |            | 100 pF    | 0603 |             |
| C2, C4                  | capacitor   |            | 10 nF     | 0603 |             |
| C5, C7                  | capacitor   |            | 1 nF      | 0603 |             |
| C10, C15, C16, C17, C18 | capacitor   |            | 100 nF    | 0603 |             |
| C11                     | capacitor   |            | -         | 0603 | not mounted |
| C12                     | capacitor   |            | -         | 0603 | not mounted |
| C13                     | capacitor   |            | -         | 0603 | not mounted |
| C14                     | capacitor   |            | -         | 0603 | not mounted |
| C19, C20, C21, C22, C23 | capacitor   |            | 1 $\mu$ F | 0603 |             |
| I1                      | BGA7350     |            | -         |      |             |
| JP1                     | jumper      |            | -         | JP5  | AG          |
| JP2                     | jumper      |            | -         | JP5  | BG          |
| JP3                     | jumper      |            | -         | JP2  | EN          |
| JP4                     | jumper      |            | -         | JP2  | VCCB        |
| JP5                     | jumper      |            | -         | JP2  | VCCA        |
| JP6                     | jumper      |            | -         | JP2  | VCCdig      |
| JP7                     | jumper      |            | -         | JP2  | VCM         |
| JP8                     | jumper      |            | -         | JP2  | VCMInA      |

**Table 12. List of components**See [Figure 35](#), [Figure 36](#) and [Figure 37](#).

| Component      | Description     | Conditions                 | Value       | Size | Remarks                 |
|----------------|-----------------|----------------------------|-------------|------|-------------------------|
| JP9            | jumper          |                            | -           | JP2  | VCMInB                  |
| JP10           | jumper          |                            | -           | JP2  | VCMA                    |
| JP11           | jumper          |                            | -           | JP2  | VCMB                    |
| JP12           | jumper          |                            | -           | JP2  | GND                     |
| JP13           | jumper          |                            | -           | JP2  | GND                     |
| JP15           | jumper          |                            | -           | JP3  | VoutA                   |
| JP16           | jumper          |                            | -           | JP3  | VoutB                   |
| L1, L2, L3, L4 | inductor        | $f_{IF} = 140 \text{ MHz}$ | 150 nH      | 0603 | dependent on PCB layout |
|                |                 | $f_{IF} = 172 \text{ MHz}$ | 100 nH      | 0603 | dependent on PCB layout |
|                |                 | $f_{IF} = 230 \text{ MHz}$ | 56 nH       | 0603 | dependent on PCB layout |
| R1             | resistor        |                            | 10 $\Omega$ | 0402 |                         |
| R2             | resistor        |                            | 10 $\Omega$ | 0402 |                         |
| R3             | resistor        |                            | 10 $\Omega$ | 0402 |                         |
| R4             | resistor        |                            | 10 $\Omega$ | 0402 |                         |
| R5             | resistor        |                            | 10 $\Omega$ | 0402 |                         |
| R6             | resistor        |                            | 10 $\Omega$ | 0402 |                         |
| R7             | resistor        |                            | 10 $\Omega$ | 0402 |                         |
| R8             | resistor        |                            | 10 $\Omega$ | 0402 |                         |
| R9             | resistor        |                            | 10 $\Omega$ | 0402 |                         |
| R10            | resistor        |                            | 10 $\Omega$ | 1206 |                         |
| R11            | resistor        |                            | 10 $\Omega$ | 0402 |                         |
| R12            | resistor        |                            | 0 $\Omega$  | 0402 |                         |
| R13            | resistor        |                            | 10 $\Omega$ | 1206 |                         |
| R14            | resistor        |                            | 10 $\Omega$ | 0402 |                         |
| R15            | resistor        |                            | 10 $\Omega$ | 0402 |                         |
| R16            | resistor        |                            | 10 $\Omega$ | 0402 |                         |
| R17            | resistor        |                            | 10 $\Omega$ | 0402 |                         |
| R18            | resistor        |                            | 0 $\Omega$  | 0402 |                         |
| R19            | resistor        |                            | 0 $\Omega$  | 0402 |                         |
| R20            | resistor        |                            | 0 $\Omega$  | 0402 |                         |
| R21            | resistor        |                            | 0 $\Omega$  | 0402 |                         |
| R22            | resistor        |                            | 0 $\Omega$  | 0402 |                         |
| R23            | resistor        |                            | -           | 0402 | not mounted             |
| R24            | resistor        |                            | 0 $\Omega$  | 0402 |                         |
| R25            | resistor        |                            | 0 $\Omega$  | 0402 | not mounted             |
| R26            | resistor        |                            | -           | 0402 |                         |
| S1             | DIP-switch      |                            | -           |      | CTS-219-05              |
| S2             | DIP-switch      |                            | -           |      | CTS-219-05              |
| S3             | DIP-switch      |                            | -           |      | CTS-219-02              |
| TR1            | 1:3 transformer |                            | -           |      | Mini Circuits ADT3-1T+  |

**Table 12.** List of componentsSee [Figure 35](#), [Figure 36](#) and [Figure 37](#).

| Component | Description     | Conditions | Value | Size | Remarks                |
|-----------|-----------------|------------|-------|------|------------------------|
| TR2       | 1:4 transformer |            | -     |      | Mini Circuits ADT4-1T+ |
| TR3       | 1:3 transformer |            | -     |      | Mini Circuits ADT4-1T+ |
| TR4       | 1:4 transformer |            | -     |      | Mini Circuits ADT3-1T+ |
| X1        | -               |            | -     |      | not mounted            |
| X2        | SMA-connector   |            | -     |      | BOUT_P                 |
| X3        | SMA-connector   |            | -     |      | BIN_P                  |
| X4        | SMA-connector   |            | -     |      | AIN_P                  |
| X5        | SMA-connector   |            | -     |      | AOUT_P                 |

12. Package outline

HVQFN32: plastic thermal enhanced very thin quad flat package; no leads;  
32 terminals; body 5 x 5 x 0.85 mm

SOT617-1

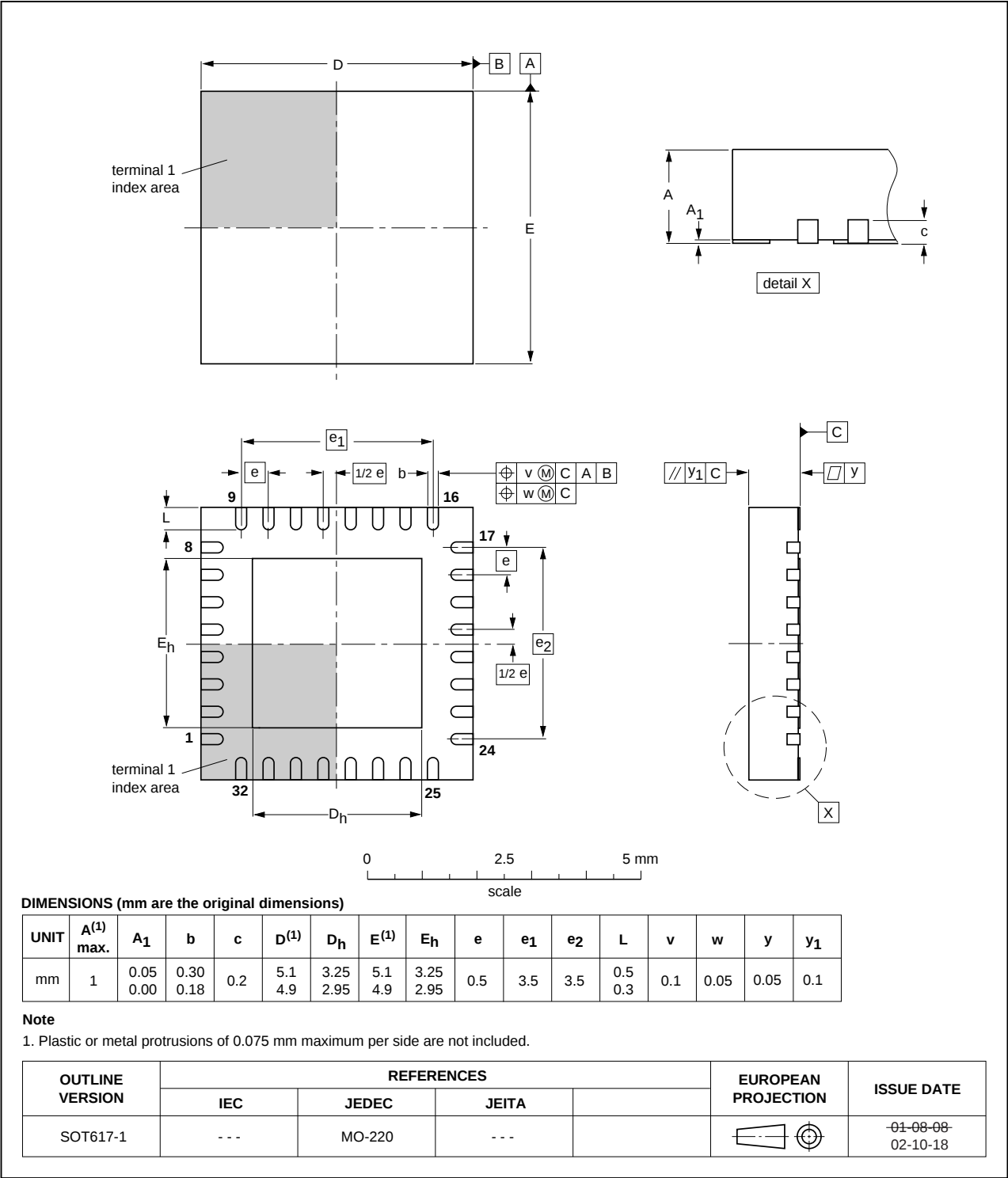


Fig 38. Package outline SOT617-1 (HVQFN32)

## 13. Abbreviations

Table 13. Abbreviations

| Acronym | Description                                     |
|---------|-------------------------------------------------|
| ADC     | Analog-to-Digital Converter                     |
| DC      | Direct Current                                  |
| DIP     | Dual In-line Package                            |
| EMI     | ElectroMagnetic Interference                    |
| ESD     | ElectroStatic Discharge                         |
| GSM     | Global System for Mobile Communications         |
| HTOL    | High Temperature Operating Life                 |
| HVQFN   | Heatsink Very-thin Quad Flat-pack No-leads      |
| IF      | Intermediate Frequency                          |
| LSB     | Least Significant Bit                           |
| LTE     | Long Term Evolution                             |
| MMIC    | Monolithic Microwave Integrated Circuit         |
| MSB     | Most Significant Bit                            |
| PCB     | Printed-Circuit Board                           |
| RF      | Radio Frequency                                 |
| SMA     | SubMiniature version A                          |
| WiMAX   | Worldwide Interoperability for Microwave Access |
| W-CDMA  | Wideband Code Division Multiple Access          |

## 14. Revision history

Table 14. Revision history

| Document ID | Release date | Data sheet status  | Change notice | Supersedes |
|-------------|--------------|--------------------|---------------|------------|
| BGA7350 v.1 | 20111221     | Product data sheet | -             | -          |

## 15. Legal information

### 15.1 Data sheet status

| Document status <sup>[1][2]</sup> | Product status <sup>[3]</sup> | Definition                                                                            |
|-----------------------------------|-------------------------------|---------------------------------------------------------------------------------------|
| Objective [short] data sheet      | Development                   | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet    | Qualification                 | This document contains data from the preliminary specification.                       |
| Product [short] data sheet        | Production                    | This document contains the product specification.                                     |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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